WHAT IS CLAIMED IS:

1. A mask pattern for multiple exposure for forming a resist pattern with an unvarying pattern pitch on a semiconductor wafer, which is utilized as in case where a mask pattern under a design having the width of an aperture pattern smaller than the width of a light-shielding pattern is used at one exposure, wherein the mask pattern for multiple exposure has a pattern pitch that is the same as that of the mask pattern under design and has the width of an aperture pattern greater than the width of a light-shielding pattern.

2. The mask pattern according to Claim 1, wherein the mask pattern is formed of chrome.

3. The mask pattern according to Claim 1, wherein the mask pattern is formed of silicon.

4. The mask pattern according to Claim 1, wherein the aperture pattern is formed using a halftone mask that becomes a phase shifter.

5. The mask pattern according to Claim 1, wherein the aperture pattern is formed using a Levenson mask that becomes a phase shifter.

6. The mask pattern according to Claim 1, wherein the light-shielding pattern is formed by using a binary mask made of chrome.

7. The mask pattern according to Claim 1, wherein the light-shielding pattern is formed by using a halftone mask made of MoSiO.

8. A method for forming a resist pattern comprising: a step for exposuring a resist on a semiconductor wafer using the mask pattern of claim 1, a step for shifting the semiconductor wafer or the mask pattern by a microscopic amount, both of the above two steps being

repeated at a plurality of times, and a step for removing a region of the resist where multiple exposure has been undergone by developing at the time when a resist pattern with an unvarying pattern pitch is formed.

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